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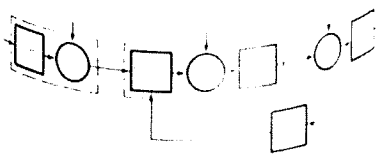
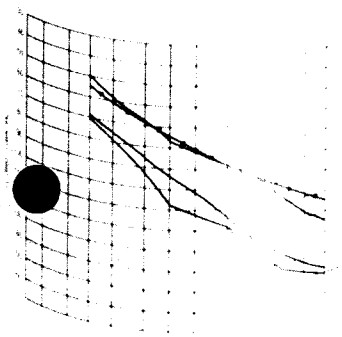
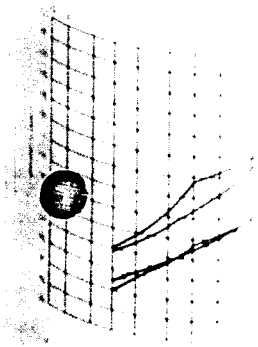
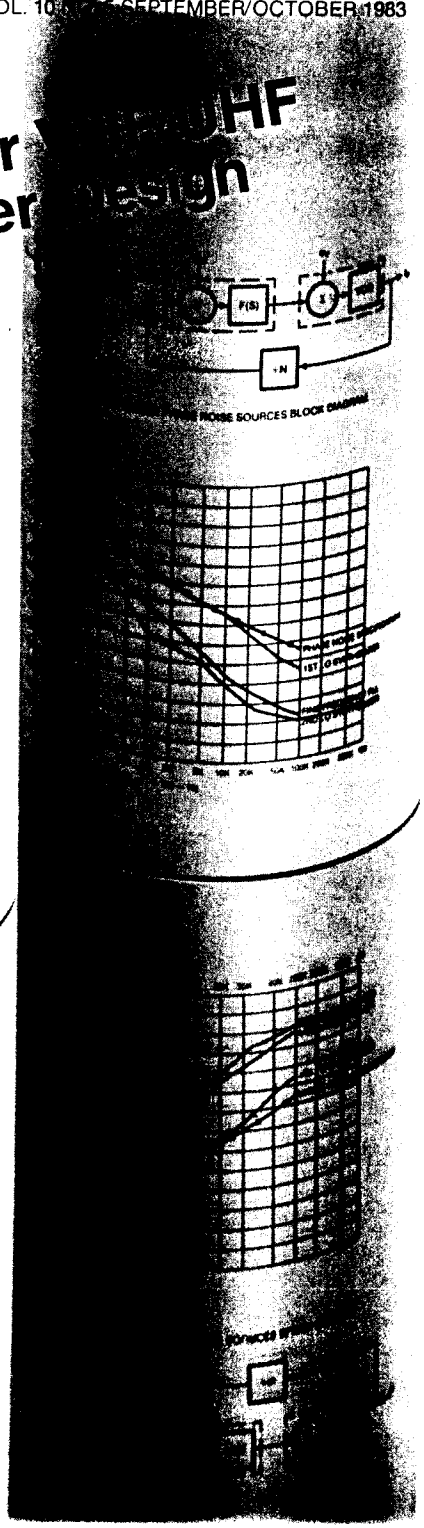
Low-Power UHF Synthesizer Design









Tech-notes

Introduction

Frequency synthesizers are crucial elements in modern communications receivers; their performance can enhance or limit overall receiver effectiveness. Phase noise is a principle measure of synthesizer performance. This article provides the reader with a background in phase-noise sources and estimating techniques, and leads into the discussion of a specific synthesizer design. Design goals and circuit implementation are also discussed. Measurements are presented to show design results and areas for improvement. Following the measurements is a brief discussion of synthesizer-performance effects on the overall receiver.

Phase-Lock Loop Background

Synthesizers, as do all phase-lock loops (PLL), have many sources of phase noise. The three sources discussed here are shown in Figure 1. They are frequency-reference phase noise (e_R), phase-detector and loop-filter noise (e_{nT}), and voltage-controlled oscillator (VCO) phase noise (e_V). Estimating the impact of these phase-noise sources is important in the initial stages of a synthesizer design. Estimates are also valuable for comparing or evaluating existing designs.

Frequency-reference phase-noise spectrum information can be gleaned from reference-oscillator data sheets. Phase-noise information is typically provided by a graph of the single-sideband phase-noise spectral density, L (f), with dimensions dBc/Hz. This data and the divider ratio, R, allow the reference oscillator phase-noise spectrum to be translated to the divider output. The governing relationship is, 20 log (1/R). Note, however, that a finite lower limit to e_R exists regardless of how large R becomes. This lower limit is determined by the technology used in the divider. The counter division ratio, R, the counter technology, and the reference-oscillator phase-noise spectrum all have to be taken into account to minimize frequency-reference effects on overall synthesizer noise.

Phase-detector output and loop-filter input noise are modeled as one source, e_{nT}. This often-overlooked source is usually the limiting phase-noise contributor inside the synthesizer's loop bandwidth. A technique for estimating the effect of e_{nT} is obtained by taking the Laplace transform transfer function from e_{nT} to the synthesizer output. Since the area of interest is inside the loop bandwidth, the obtained transfer function can be simplified to:

$$L(f_m) = 20 \log \frac{NE_{nT}(f_m)}{K_p} \text{ dBc/Hz}$$

$E_{nT}(f_m)$ is the loop-filter input equivalent noise-voltage spectrum ($V/\sqrt{Hz}$),

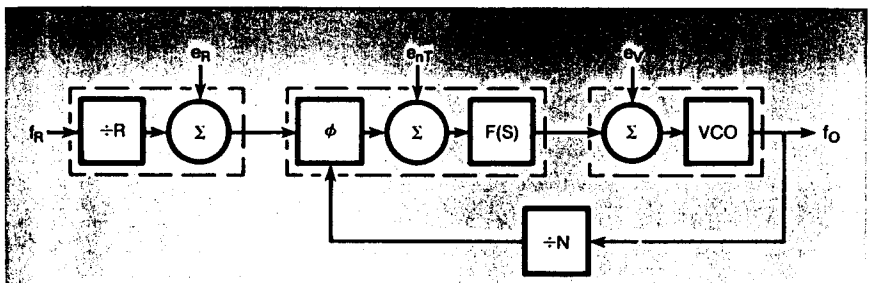


Figure 1. Synthesizer phase-noise sources block diagram.

which can be obtained from manufacturer data sheets. The phase-detector gain constant, K_p, in V/radian is the detector output-voltage range divided by its range in radians. Note that the above equation does not contain the loop gain, but only N, E_{nT} and K_p. Therefore, to reduce the contribution of this noise source to the synthesizer-output phase noise, three measures can be taken:

1. select a different frequency plan that allows a lower division ratio, N.
2. choose a lower input-equivalent noise-voltage loop amplifier.
3. use a higher-gain phase detector.

The first two options are straightforward, therefore, only the third will be discussed in detail.

Gain constants vary with the type of phase detector. A popular TTL digital phase/frequency detector has an output swing of 1.5 volts and a range of 4π radians; therefore, it has a gain constant of 0.12 volts/radian. A similar CMOS circuit has a gain constant of 0.4 volts/radian when operating from a 5-volt supply, or 0.72 volts/radian when operated at 9 volts. A discrete circuit sample-and-hold phase detector operating with a 10-volt output swing has a gain constant of 2.0 volts/radian. Comparing the phase-detector constants, a 24-dB phase-noise improvement is realized by selecting the sample-and-hold detector over the TTL phase/frequency type. It is also seen that the CMOS circuits offer performance between these two extremes.

Estimating the VCO contribution to synthesizer phase noise requires knowledge of the frequency range (ΔF) and the available tuning voltage range (ΔV). This information is used to calculate the VCO gain constant, K_{VCO} (MHz/volt):

$$K_{VCO} = \frac{\Delta F + M}{\Delta V} \text{ MHz/volt}$$

M = frequency overlap or design margin.

Next, assume a residual noise voltage, E_n, riding on the VCO tuning voltage input. E_n and K_{VCO} are then used to calculate the VCO's incidental frequency modulation (IFM):

$$IFM = K_{VCO} E_n \quad \text{Hz in 1-Hz bandwidth}$$

A realistically achievable lower limit for E_n is 0.1 μV. The VCO phase-noise spectrum is then obtained by using:

$$L(f_m) = 20 \log \frac{IFM}{\sqrt{2}\ f_m} \text{ dBc/Hz}$$

Looking at these relationships, only two ways to improve phase noise are noted: Lowering the value assumed for E_n, which, in an actual system may be impossible, or reducing K_{VCO}. The VCO gain constant, K_{VCO}, can be lowered by increasing the available tuning-voltage range or by reducing the oscillator frequency range. These last two parameters are not usually at the sole discretion of the synthesizer designer, since power supply voltage and other system limitations may apply. However, using band switching in the VCO accomplishes the desired reduction of K_{VCO}. A limit on the number of band switches, however, is imposed by physical circuit limitations. These limitations are imposed by layout constraints and/or the losses associated with the band-switching circuitry.

The discussion of PLL phase-noise sources provides a model for looking at synthesizer phase noise and techniques for making estimates. These techniques are simplified and must be expanded for an actual design. They can, however, be used for quick comparisons between designs and for looking at the effects of circuit trade-offs within a design. Starting with these simple

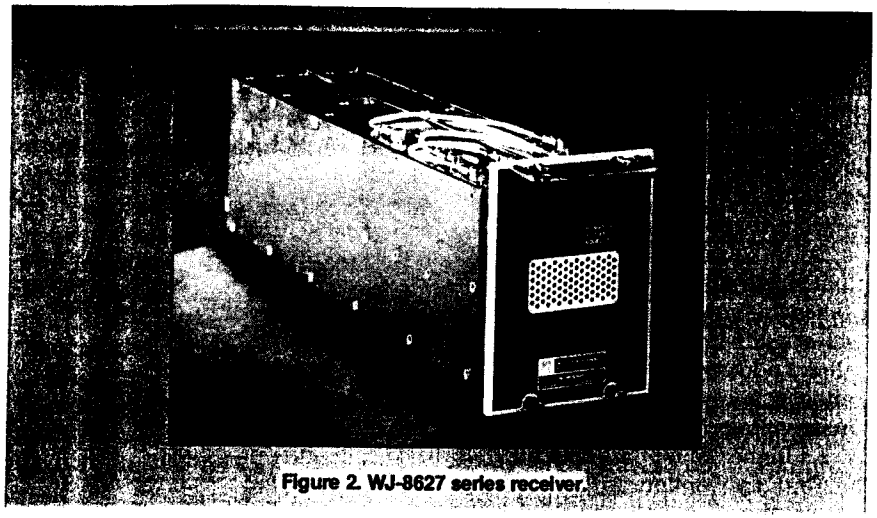


Figure 2. WJ-8627 series receiver.

estimation techniques, the low power, low phase-noise synthesizers of the WJ-8627 series receivers were designed. A typical WJ-8627 receiver is shown in Figure 2.

Design Goals

Design goals established for the new series of receivers include low power consumption, improved performance, commonality between units and circuit simplicity.

A goal of one-half the power consumption of the existing design was set. Therefore, all design decisions were made with power as a primary concern. Higher-efficiency amplifiers were considered, new low-power technology explored, and frequency plans evaluated for their impact on power consumption.

The performance improvement goal was characterized by a 45-dB FM ultimate signal-to-noise ratio (S/N) specification, with no video bandwidth restricting filtering (less than B/2 cutoff). This related directly to a more stringent synthesizer phase-noise requirement. The relationship between receiver incidental frequency modulation and measured FM ultimate S/N, shown below, was used.

$$\Delta f_{RMS} = \frac{.707(.3B)}{10^{\frac{S/N}{20}}} \quad \text{Hz in a B-Hz bandwidth}$$

Δf_{RMS} = incidental frequency modulation in a specified bandwidth, B.

B = IF bandwidth in Hz

The Δf_{RMS} value was then linked to the single-sideband phase-noise spectrum, L (f_m), by the following equation, evaluated with f_m equal to the IF band-edge (B/2):

$$L(f_m) = 20 \log \frac{\Delta f_{RMS}}{\sqrt{2}\, f_m \sqrt{B/2}} \text{ dBc/Hz}$$

This point and a -20 dB/decade line through it define the required phase-noise performance for a given S/N goal. Improved FM detector and video circuitry capable of sustaining the 45-dB level is also required.

Commonality of circuitry designs, printed-circuit boards, chassis, and frequency plans increase potential manufacturing flexibility and reduce maintenance training. The use of similar circuits increases production, field technicians' familiarity with the various WJ-8627 series receivers, and is also greatly enhanced by common connector placement on all functional modules. A flexible frequency plan is required to allow the circuit commonality goal to be met.

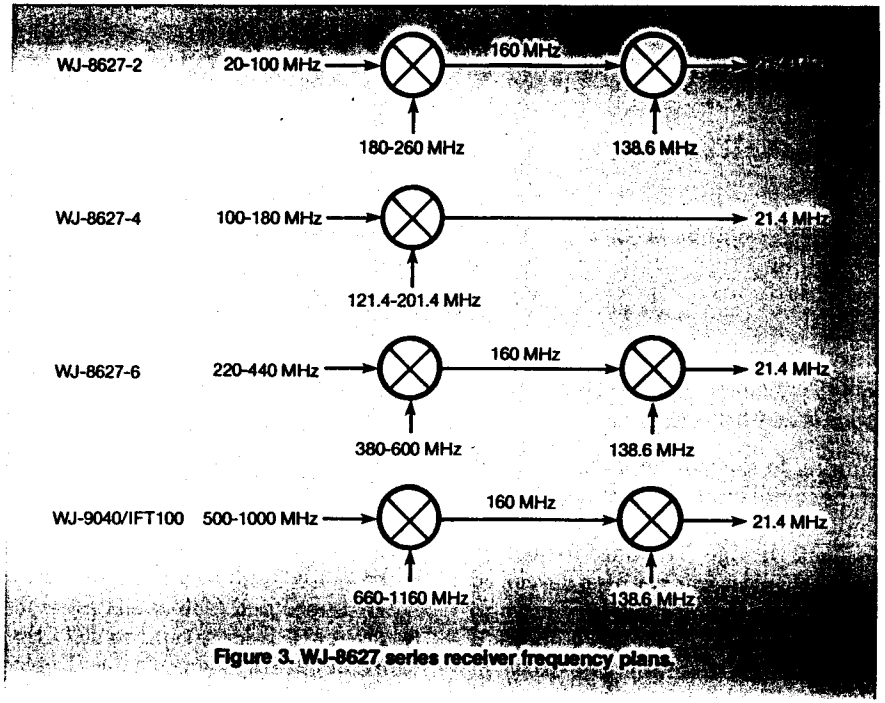


Figure 3. WJ-8627 series receiver frequency plans.

Circuit simplicity provides the long-term benefits of easy, straightforward alignment and troubleshooting, thus eliminating the requirement for highly trained personnel to handle routine maintenance.

Circuit Implementation

In designing the WJ-8627 series of receivers, trade-offs had to be made in implementing the circuitry to fulfill the goals of low power, high performance and flexibility, while still maintaining a simple design.

The frequency range to be covered was divided into four coverage bands: 20 to 100 MHz, 100 to 180 MHz, 220 to 440 MHz, and 500 to 1000 MHz. Frequency plans for each frequency band were considered individually, and then in combination, to provide maximum commonality. The final frequency plans are shown in Figure 3. The common intermediate frequencies of the dual conversion plans allow common circuits to be used in all cases. Note that a fixed 2nd local oscillator (LO) frequency is used. Synthesizing a fixed frequency has the design advantages of low power and high performance. Also, a fixed 2nd LO requires that all receiver tuning occur in the 1st LO, thus providing the flexibility to choose a single conversion frequency scheme, as in the 100-to-180 MHz band, by simply eliminating the 2nd LO. A closer look at Figure 3 reveals that the 1st LO frequencies are relatively low. Since power consumption is roughly propor-

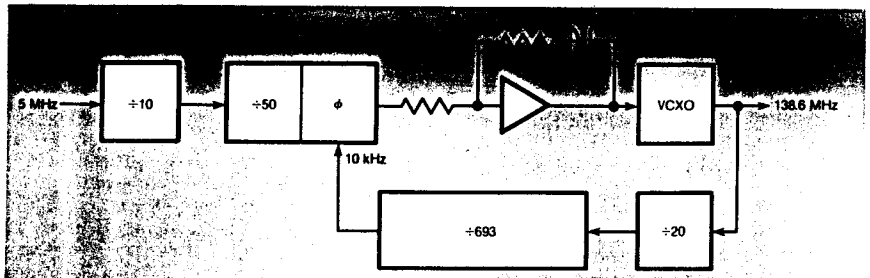


Figure 4. 2nd-LO synthesizer block diagram.

tional to frequency, low LO frequencies help conserve power.

Turning to the synthesizers, let's look at the circuit implementations that met the design goals for the 220 to 440 MHz frequency range. The fixed-frequency, 2nd-LO synthesizer has been developed around a voltage-controlled crystal oscillator (VCXO). Figure 4 shows a 2nd-LO block diagram. The excellent phase-noise performance was inherent in the 2nd-LO design. CMOS large scale integrated circuitry, coupled with low-power prescaling, resulted in minimal power consumption, and a single production adjustment provided alignment ease.

The 1st-LO synthesizer will be addressed in three major sections: the fine-frequency PLL, the upconverter, and the output PLL. A block diagram is given in Figure 5.

Some important factors of the fine-frequency PLL design are the VCO, the CMOS digital dividers, and the sample-and-hold phase detector. The low-frequency VCO provides very good phase-noise performance with low power consumption. CMOS dividers in both the reference and N_2 dividers

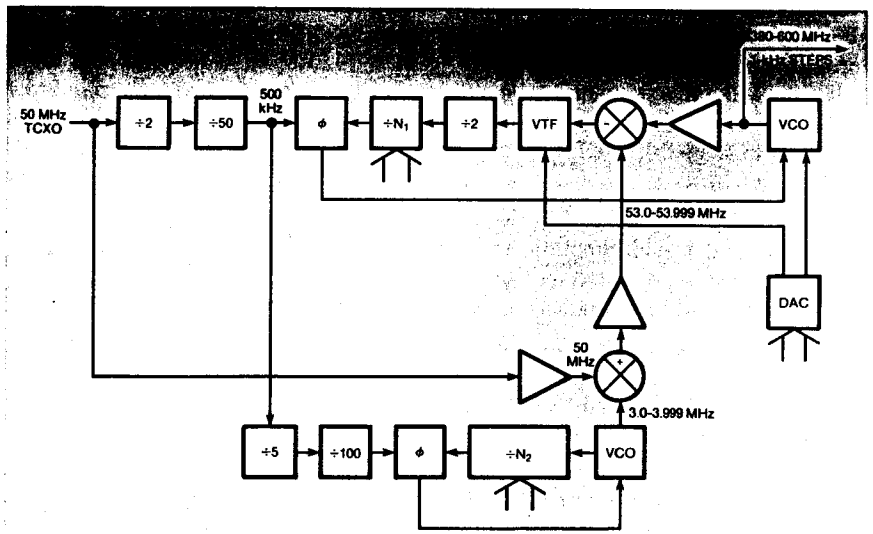


Figure 5. 1st-LO synthesizer block diagram.

greatly reduce power consumption over typical bipolar (TTL) designs. Selection of the sample-and-hold phase detector was based on its superior phase-noise and reference-sideband performance, compared to the other types discussed previously.

The upconverter circuit provides two functions. First, it allows a low-frequency, high-performance, fine-frequency PLL to be injected into the output PLL at useable frequencies. Second, it filters the unwanted mixer products to keep these spurious products from entering the output PLL. Note that the 50-MHz frequency reference oscillator is amplified and used as the upconverter LO. This provides an extremely low-noise LO without the need to generate it by more complicated means. Both amplifiers in the upconverter are designed using power amplifier techniques that enhance efficiency.

The output PLL will be presented in several parts in the following discussion: The phase detector, N_1 divider, voltage-tunable filter (VTF), digital-to-analog converter (DAC) and VCO.

A sample-and-hold phase detector is used again, not only because of its superior performance, but also to carry common circuitry in both the fine-frequency and output PLLs. This increases the similarity between both PLLs, thus lowering cost and trouble-shooting time.

Previous N_1 dividers had been large power consumers, typically 2.5-to-3.5 watts in the VHF/UHF frequency range, but design improvements enable power consumption to be reduced to 1.5 watts. The selection of an output PLL reference frequency of 500 kHz and a divide-by-2 prescaler was determined on the basis of providing the lowest power-consumption design available. Further reductions in power will become possible as the next generation of digital logic becomes commercially available.

The VTF is the key component in eliminating mixer-related spurious responses in the output PLL. It must eliminate spurious responses without adding appreciable phase shift and, therefore, instability to the PLL. Reduced labor costs are achieved by realizing all resonator coils with microstrip lines.

The DAC circuit provides coarse tuning of the VCO and the tuning voltage required by the voltage-tuned filter. Low output-noise voltage is required in these applications to reduce potential AM-to-PM conversions, which can severely degrade synthesizer phase-noise performance. CMOS integrated circuits and a band-gap reference meet the above requirements. They also consume very little power.

The output PLL VCO is the most complex and critical circuit in the 1st-LO synthesizer design. Poor performance in this critical circuit can overshadow the entire design. The specific oscillator chosen is a quarter-wave transmission-line type. Figure 6 shows a sketch of the VCO circuit. Inherent mechanical stability, low signal radiation, and the elimination of the need for a high-Q coil are factors in the oscillator selection. The multiband VCO reduces K_{VCO}, and thus, reduces phase noise. This VCO design is used in all frequency range receivers to increase circuit commonality. A five-band design is used in the 380-to-600 MHz synthesizer shown.

Performance Measurements

Performance measurements were made on a 220-to-440 MHz receiver. Total power consumption of the receiver measures 14 watts. Eight watts is dissipated in the synthesizers. Both LO

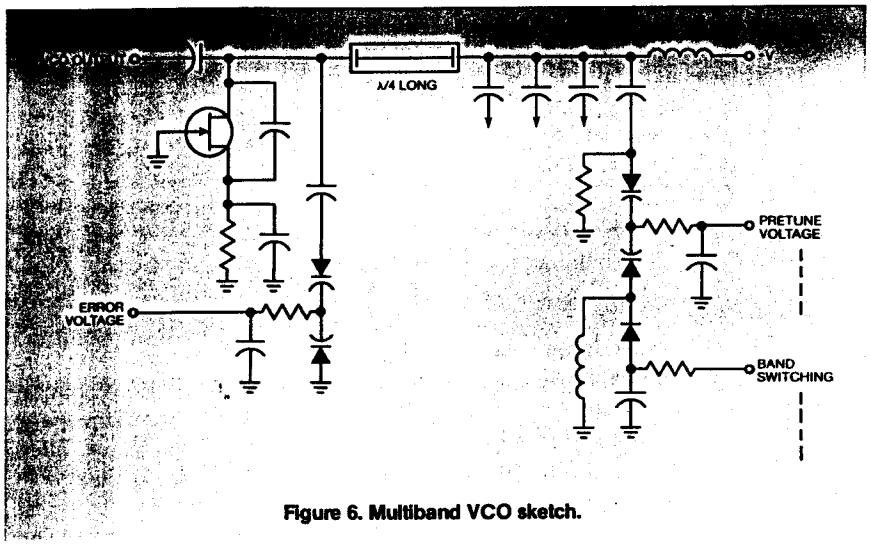


Figure 6. Multiband VCO sketch.

synthesizers are housed in a common chassis consisting of one-third the receiver volume. A free-air temperature rise of 16°C was measured in this module.

Synthesizer phase-noise performance measurements are shown in Figure 7. Measured performance for the 2nd-LO PLL, fine-frequency PLL and 1st-LO synthesizer are presented. Also shown is the required phase-noise performance derived from the 45-dB FM ultimate signal-to-noise ratio goal. Second-LO performance is 30 dB better than required. The fine-frequency PLL phase noise is approximately 20 dB below the specification. The 1st-LO synthesizer measures to the required specification. Ultimate FM measurements of 46 dB indicate that the overall receiver phase noise integrates to below the design specification.

The overall receiver phase-noise performance is determined by the 1st-LO synthesizer output PLL. Further investigation reveals that the VCO is the primary contributor. Therefore, improving the VCO phase noise directly improves receiver performance. Since the measurements were recorded on a 5-band VCO, the PLL background discussion for reducing K_{VCO} is again applicable. Adding more bands would decrease VCO phase noise. This fact has been utilized in the development of the synthesizers for the other receiver frequency bands, and better phase-noise performance has been verified.

Performance Implications

What are the implications of low power consumption and low phase-noise performance? Low power consumption allows convection cooling, thus eliminating acoustic and electrical noise, additional power, and the problems associated with mechanical vibration due to the presence of a fan. The costs associated with forced-air cooling are also eliminated. Electronic circuit reliability rapidly increases as the stress of high temperatures is reduced, thus increasing the mean time between failures and reducing maintenance costs. Lower phase-noise levels allow higher signal-to-noise ratios, thereby enhancing post-detection processing effectiveness. Reciprocal mix, which is

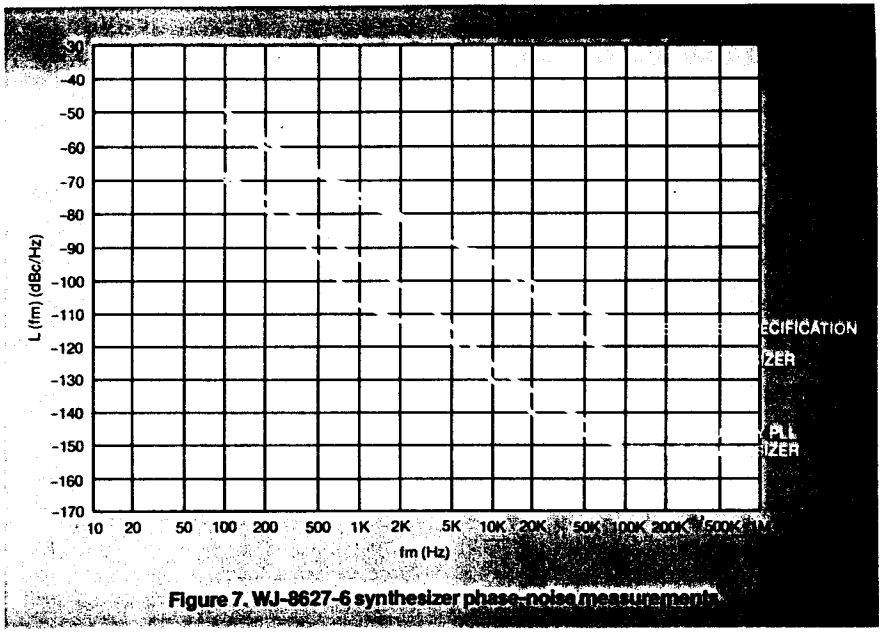


Figure 7. WJ-8627-6 synthesizer phase-noise measurements.

characterized by a loss of small-signal sensitivity in the proximity of a large signal, is also reduced.

Conclusion

A simple phase-noise model for frequency synthesizers has been presented. The phase-noise model is useful in the early stages of a synthesizer design to analyze trade-offs. This is shown in its application to comparing types of phase detectors. It is also useful in evaluating existing designs. The PLL background section is followed by a discussion of a compact-receiver synthesizer design. Design goals and implementation highlights of the WJ-8627 VHF/UHF handoff receiver series have been presented. Measured performance of a WJ-8627-6 (220-to-440 MHz) receiver synthesizer is given, and its implication to receiver performance has been briefly discussed.

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References

1. Manassewitsch, Vadim, "Frequency Synthesizer Theory and Design," John Wiley and Sons, New York, 2nd Edition 1980.
2. Grebenkemper, C. John, "Local Oscillator Phase Noise and Its Effect on Receiver Performance," Watkins-Johnson Company, San Jose, California, October 1981.
3. Martin, Larry, "Noise-Property Analysis Enhances PLL Designs," EDN, September 16, 1981.