First-Time-Right Design Of RF/Microwave Class A Power Amplifiers Using Only S-Parameters

The sequel to "Tandem RF software programs streamline the design of power amplifiers" [7]

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This article describes and discusses a procedure of how to design RF/Microwave Class A power amplifiers in a very efficient and highly accurate manner when the only initial data available are the *S-parameters* of the transistors. As in the prequel [7], two software programs are used in conjunction and interaction: a specialized RF/Microwave amplifier design software tool and a general-purpose simulator (nodal analysis program). This time the simulator is not used for its nonlinear analysis capabilities but mostly for its integrated layout EM simulation capabilities.

The *Power Parameters* Design Method

S-parameters can be used to design Class A amplifiers for optimum gain and input/output return loss at the biasing point at which the transistor *S-parameters* have been measured. If *Noise Parameters* are available and they are combined with the *S-parameters,* it also becomes possible to design for optimum Noise Figure (NF) and the associated available power gain (G_{anopt}). The *S-parameters* by themselves do not allow for controlling the output power obtained from each stage of the amplifier to be designed. The power of interest in a Class A amplifier is usually the maximum linear output power which is universally accepted to be the power at the 1dB compression point of the gain, that is, P1dB. As with the *Noise Parameters,* which are needed to control the noise performance of an amplifier, some kinds of *Power Parameters* are needed to design for P1dB.

One method of designing and analyzing for P1dB is to use non-linear transistor models and non-linear (harmonic-balanced) simulators. The biggest problem here is that non-linear models are often not readily available. The manufactures of transistors rarely provide them, and the equipment and software that can be used to extract the non-linear models are very expensive and few companies can afford them. The same applies to the method of using tuners to extract the optimum input and output impedances, or the load-pull constant power contours of the transistors. Of course these methods are unavoidable when very heavy non-linear modes of operation are used and information for the signal distortion is needed.

Cripps, in his usual manner of defying the “conventional wisdom”, introduced and developed in [2], [3] and [4] a simple approach for estimating and designing for the maximum output power of mildly non-linear (Class A) power stages. In this approach the transistor is approximated by a very simple equivalent model consisting of the intrinsic voltage controlled current source (generator) and the parasitic output parallel capacitor and series inductor. The weakly non-linear effects are ignored and the transconductance is considered to be linear until the voltage across it and/or the current supplied by it clips strongly when voltage pinchoff and/or current saturation is reached. Under these assumptions, Cripps developed linear mathematical expressions, which tie together the load-line and the voltage and current limits across the intrinsic generator with the external load and the output power delivered to this load. He showed how to present the relation between the intrinsic load-line and the external impedance on a Smith Chart as constant output power (load-pull) contours.

The *Cripps Approach* became very popular because of its simplicity and the satisfactory results it provides in many cases. The simple three-element equivalent model can easily be extracted when a full linear equivalent circuit is fitted to the *S-parameters* of the particular transistor. This approach is, however, often not general enough. Some of its limitations are that it does not allow for feedback or transistor losses. In [3] Cripps pointed out that it is a simple task to implement the equations presented in the article into a linear simulator to simulate the power performance in the same manner that most simulators compute noise figure. He also pointed out that, with a slightly more innovative approach, the effect of the feedback could also be taken in account.

The *Cripps Approach* can be considered to be the basis for the *Power Parameters* introduced by Abrie in [1] and described more thoroughly in [5]. Abrie used mathematical mapping functions to relate “the intrinsic voltages to the external voltages and the intrinsic output current”. This innovation takes away (lifts) in a very elegant manner all the limitations of the *Cripps Approach.* The *Power Parameters* take in account feedback and losses, as well as changes in the transistor configuration. This makes their application universal and allows for most versatile amplifier design. The *Power Parameters* allow P1dB of each stage in multistage amplifier designs to be controlled and analyzed in relation to the other stages. Interestingly enough the *Power Parameters* behaviour resembles the *Noise*

Parameters behaviour. P1dB is independent of the source impedance, while NF is independent of the load impedance. Feedback (series or parallel) affects P1dB in a similar manner as NF. *Power Parameters*, however, have one distinctive advantage on the *Noise Parameters*: They do not require measurement with special and expensive equipment and tedious setup and measurement procedures. The only information required is the linear model of the transistor, the bias point, the I/V curves boundaries and the slopes of these boundaries (if available). If a small-signal model is not available, the required model can usually be extracted easily from the *S-parameters.*

The Software Tools

Power Parameters can be implemented or added into any linear simulator, but for the time being they are available only in *MultiMatch Amplifier Design Wizard. MultiMatch* is specifically dedicated to the design of amplifiers and oscillators. It combines linear frequency domain simulation and iterative synthesis of passive networks. Two kinds of passive networks can be synthesized. The first type is *modification networks* as they are defined in *MultiMatch.* The *modification networks* usually contain resistors and they could be either loading the transistor or they could be feedback sections (series or parallel). Loading and feedback can of course also be simultaneously implemented. The other kind of synthesis is for purely reactive, lossless matching networks. The control parameters for the synthesis of the passive networks are the requirements for gain, return loss, stability, noise figure, P1dB, oscillator start-up frequency and tuning range, etc. The design procedures are actually set up to synthesize amplifiers or oscillators, not just passive networks.

MultiMatch allows linear power amplifiers to be designed very efficiently, but in order for the design to produce *first-time-right* results, additional special care must be taken of the discontinuities of the matching networks designed for high power RF transistors, as is emphasized in [6]. That can be done by using MultiMatch in conjunction with a nodal analysis simulator, which incorporates layout EM simulation. As in [7], *Microwave Office* was chosen for the designing the amplifier considered here. Some of the reasons for choosing *Microwave Office* are that before everything it is very user-friendly and, with its Application Programming Interface, it provides the possibility for seamless interaction with other software tools. In this case *MultiMatch* exports its schematics into script files that can be executed inside *Microwave Office* to translate the *MultiMatch* schematics into *Microwave Office schematics.*

The Design Problem

It was necessary to develop a 5W Class A single-ended amplifier stage for the 2.1-2.2 GHz frequency band with gain of 10-11dB. The single-ended stage was subsequently used to configure a balanced 10W amplifier stage. The transistor chosen was the Mitsubishi MGF909A which delivers a minimum of 37dBm of P1dB at the biasing point of 10V, 1.3A. Mitsubishi provides *S-parameters* for this bias point but does not offer any nonlinear model or load-pull data for the transistor.

The Design Procedure

The design started in *MultiMatch.* A design bandwidth of 2.075-2.225 GHz with a step of 25MHz was set up; substrate parameters were entered, etc. Then a command for modifying a transistor was invoked (Figure 1).

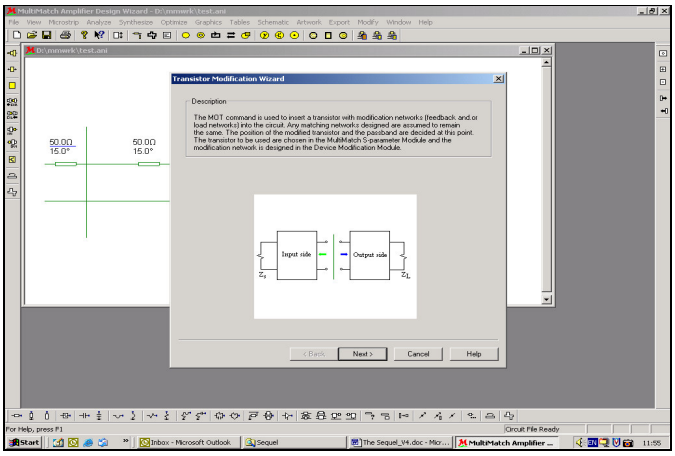

Figure 1. Transistor modification starting window

The first thing to be done when designing for P1dB is to fit a linear model to the *S-parameters* the transistor. Figure 2 shows the window dedicated to this purpose. The measured *S-parameters* and the parameters associated with the model fitted are compared in Figure 3. Note the optimization facility in Figure 2 and the option to display the graph mentioned. The bias point (dc operating point) and the I/V Curve Boundaries are also specified at this point. With a model fitted and the load-line boundaries specified, *MultiMatch* can calculate the *Power Parameters* and predict and synthesize for P1dB.

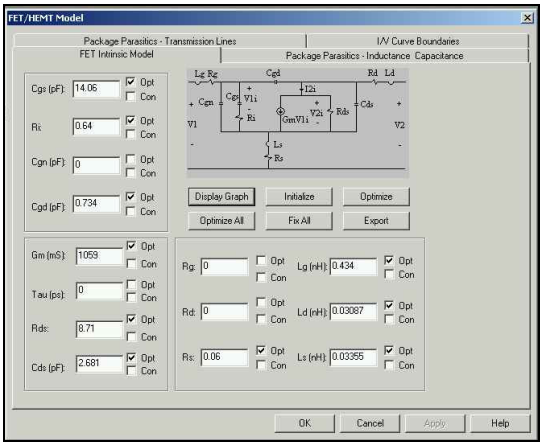

Figure 2. Transistor model fitting facility

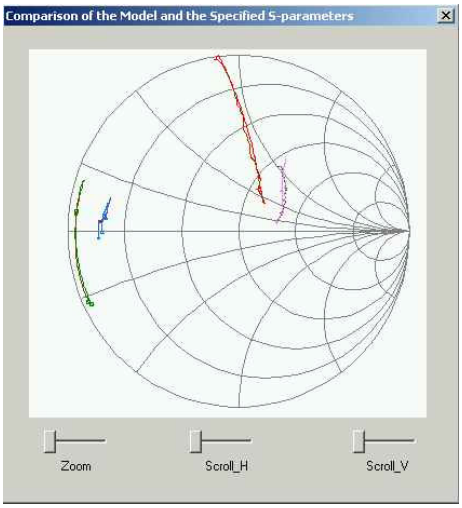

Figure 3. Graph showing the result of the fitting

The next step was to do a general analysis of the transistor capabilities. This showed that the maximum P1dB that can be achieved is close to 38dBm and that the gain could be up to 13dB when the output is matched for maximum P1dB. The *k-factor* (Rollette stability factor) of the transistor shows that the transistor is unconditionally stable above 1.8GHz and becomes less and less stable towards lower frequencies. At this stage of the design, it is possible to guide *MultiMatch* to synthesize modification networks at the input that would contain resistors and that would stabilize the transistor, level the gain and pre-match the transistor. The modification networks can, however, be a bit tricky to realize physically with surface-mount components at the input of the transistor when the transistor has very low input impedance. It was decided to get out of the modification section, proceed to synthesis of output and input matching networks and then add at the very input a network to provide the required stability at the low frequencies.

The next action was to execute the command that starts the synthesis of output networks for the particular transistor stage. The *MultiMatch Amplifier Design Wizard* goes through a sequence of

specification (setting-up) windows in an interactive dialogue with the designer. The dialog boxes for specifying the target load-pull P1dB contours are shown in Figures 4 and 5. Then follow dialogue boxes with tables (not shown here) from which the impedances to be used to extract the required P1dB can be selected (The power remains the same around any target contour, but the other parameters of interest will vary).

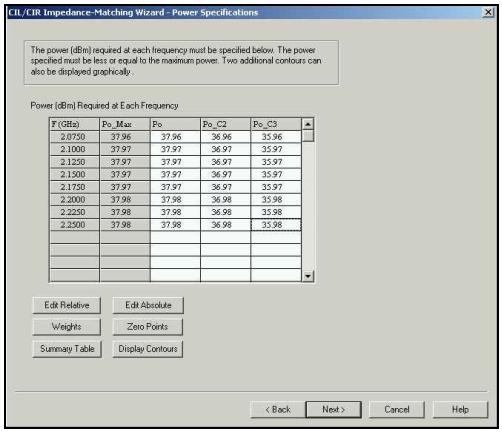

Figure 4. Load-pull contours set-up window

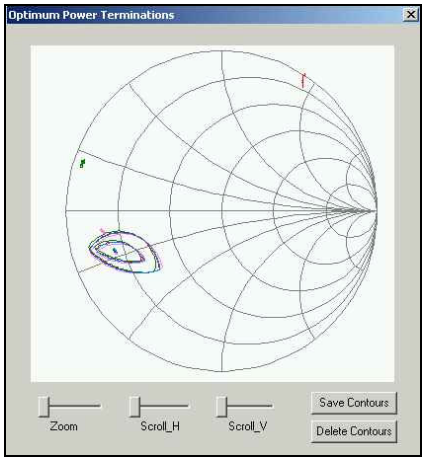

Figure 5. Load-pull contours

In this case *MultiMatch* was instructed to select the impedances for the maximum P1dB. With the target load terminations defined, *MultiMatch* switched to the Synthesis Section Menus and the syntheses of the output matching network was initiated. The synthesis of the matching networks is done again in an interactive mode between the program and the designer (It could take quite a few trials before a satisfactory solution is found). At this stage of the design process the designer should also start worrying about the effect of the discontinuities in the microstrip network that would be synthesized. The first few synthesis trials were done just to get an estimate of the most problematic discontinuities and how to approach solving the problems that they would create. It became obvious that the biggest discontinuity would be the step between the output pin of the transistor (0.6mm) and the first low-impedance transformation line (13.4 Ω, 10 mm width). It was decided to first simulate this step in the EM layout simulator of *Microwave Office.* Figure 6 shows the EM simulation of the step and the current distribution in it. The current distribution reveals where the discontinuity is actually taking place and this was taken in account when the two reference planes were placed for the extraction of the *S-parameters* of the step (see Figure 7).

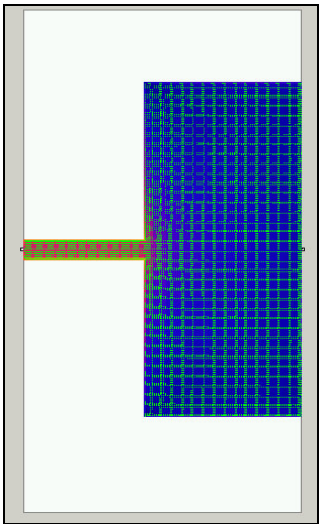

Figure 6. EM step with current distribution

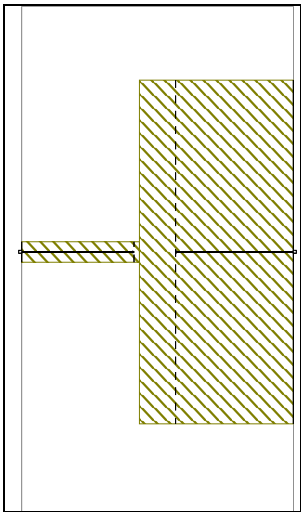

Figure 7. Reference planes of the step

The *S-parameters* of the step were imported into *MultiMatch* (Figure 8) and the synthesis of the output network for maximum P1dB was started again. The synthesized solution is given in Figure 9 in schematic form and in layout form in Figure 10.

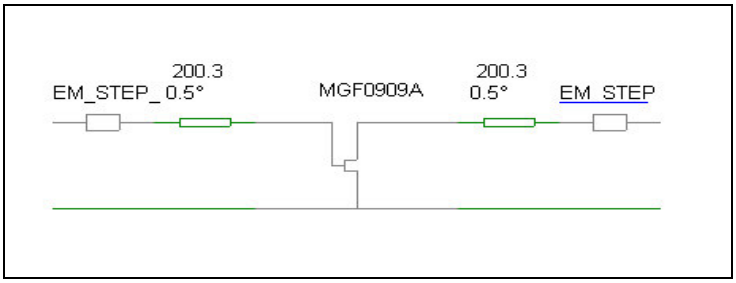

Figure 8. EM simulated step added to the input and output of the transistor

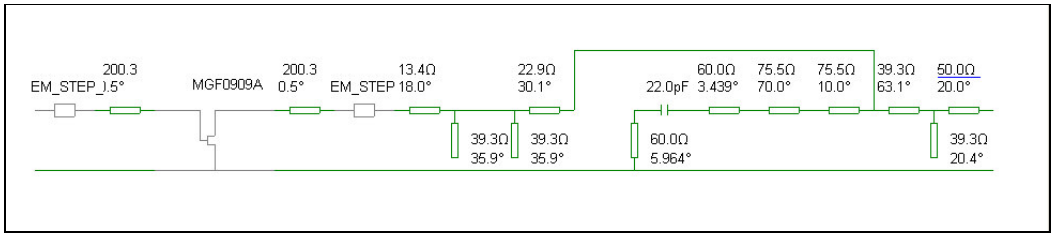

Figure 9. The synthesized output network added at the output of the transistor

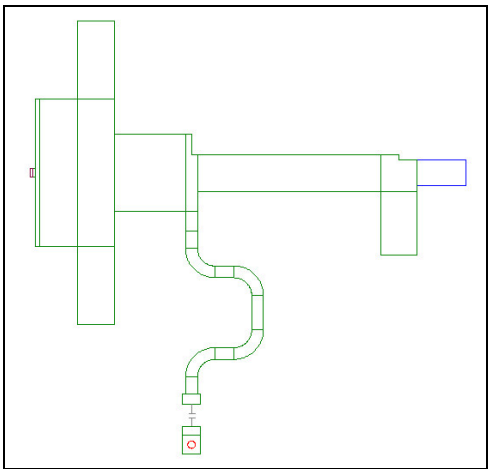

Figure 10. The layout of the output matching network

The high impedance parallel stub terminated with a capacitor to ground was not part of the synthesized solution. It was added manually for biasing purposes and it's about 90° long at the middle of the frequency band.

The synthesis of the input matching network for maximum gain was performed in a very similar manner. A stabilizing network consisting of a resistor and shorted (by capacitor) stub was added at the very input as was mentioned above and serves as a biasing network too. The layout for the full amplifier stage generated by *MultiMatch* is presented in Figure 11.

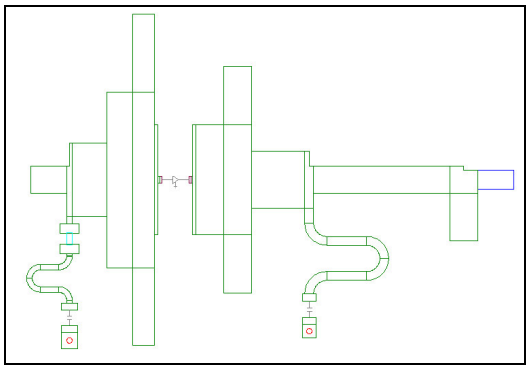

Figure 11. MultiMatch generated amplifier layout

The description of the synthesis procedures was omitted here but it was fairly well described in [7]. The simulation of this solution shows that P1dB should be expected to be more than 37.5dBm over the design frequency band. The gain and input and output return loss are shown in Figure 12. In order to present the results from different simulation in the same format the graph in Figure 12 is from *Microwave Office* but it is a *MultiMatch* simulation imported as *S-parameters.*

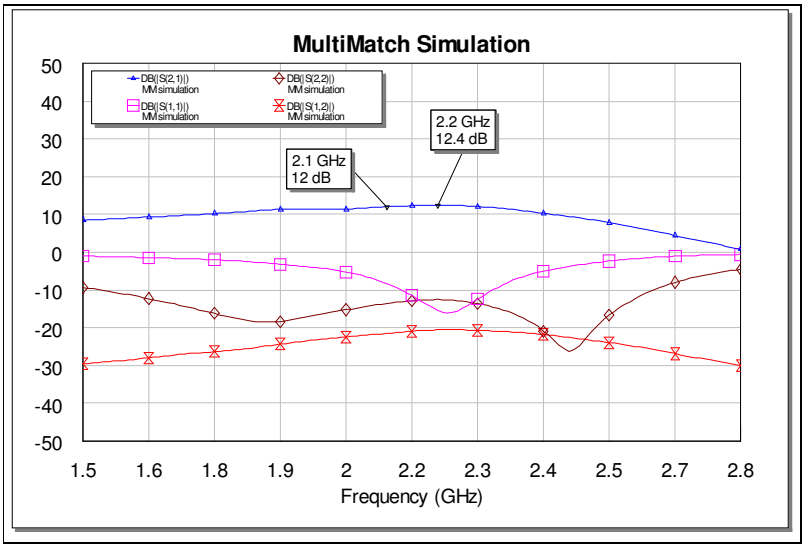

Figure 12. *MultiMatch* gain and return loss simulation

Although the most significant discontinuity was taken in account already, the rest of the discontinuities in the input and output matching networks are still out of the range of any of the existing models for discontinuities. In order for their effect to be tuned out, the design was continued in *Microwave Office*. In order to remove the parasitic influence of the discontinuities, the output network in the *MultiMatch* analysis file was isolated and, after simulation in MultiMatch, its *S-parameters* were imported into *Microwave Office*. The schematic of the output network was then also imported into *Microwave Office (Figure 14)*. The corresponding layout is show in Figure 15.

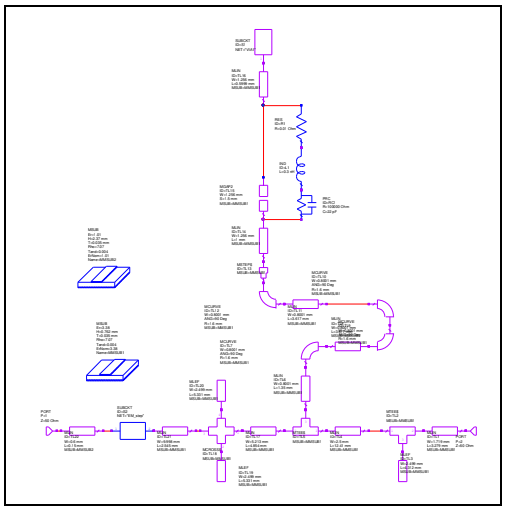

Figure 14. Output matching network schematic in *Microwave Office.*

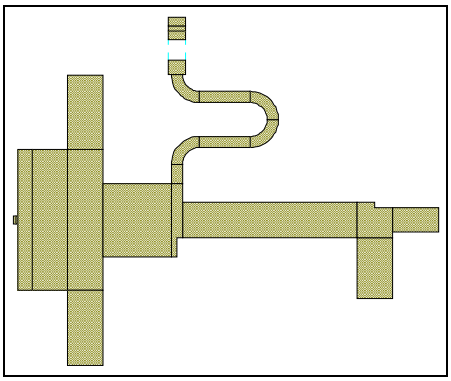

Figure 15. The corresponding layout

The part of the layout without the curved lines section was simulated in the EM simulator and its *S11* was compared with the *S11* of the *S-parameters* that were imported from the simulation in *MultiMatch.* The slight difference was tuned out by changing some of the dimensions of the EM simulated structure. This can be done easily and quickly in the user-friendly environment of *Microwave Office.* In Figure 16 the red trace on the Smith Chart shows the simulation from *MultiMatch*, the green trace is the simulation with the EM section of *Microwave Office* before tuning and the blue trace is after tuning. It could be a good idea to remind the reader that it is the *S11* of the output matching network that defines the P1dB of the transistor stage. In this case the highest P1dB obtainable from the transistor is targeted.

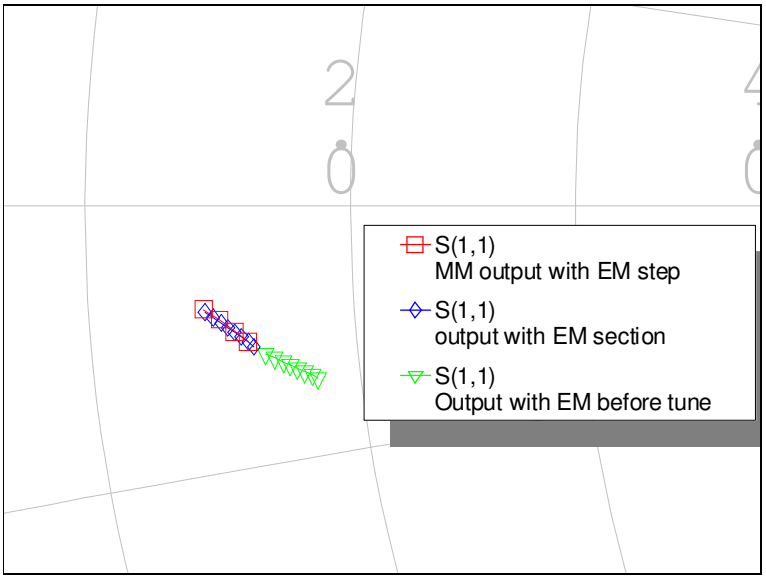

Figure 16. *S11* of the output matching network

Figure 17 compares the layouts of the section of the output network that was EM simulated before and after tuning (the green and the blue trace in Figure 16).

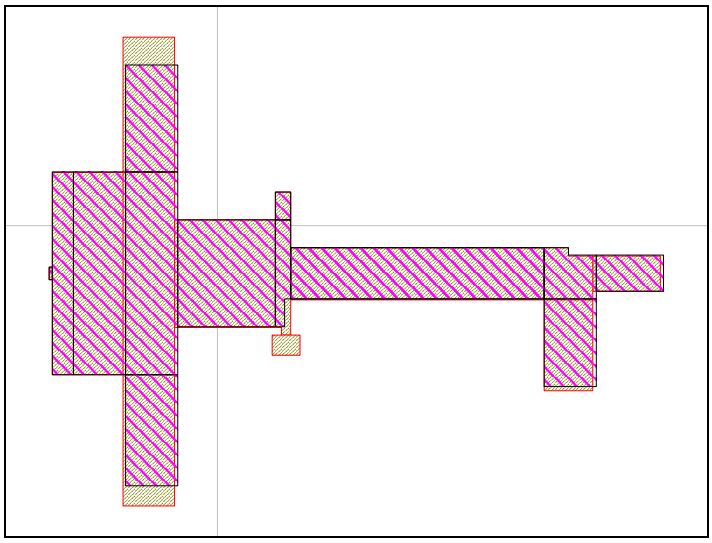

Figure 17. EM simulated output network sections before and after tuning

A question may arise here as to why was it necessary to include the effect of the step upfront in *MultiMatch* before synthesis of the network when it is analyzed again in the EM structure shown in Figure 17. Experience has shown that without doing this, the simulated *S11* before tuning (green trace) will be much farther away from the target (red trace) and it would be not possible to tune it easily and without some major changes to the layout, or it would be not even possible to tune it for the whole bandwidth.

The same approach was used to EM tune the input matching network but this time the tuning criteria was to achieve maximum gain for the amplifier, instead of targeting the *MultiMatch* performance. The final RF layout is shown in Figure 18. The DC part of the layout was added in another drafting software, the PCB was produced and a test unit (Figure 20) was built and measured. Figure 19 shows the gain and the return loss of the simulation of the amplifier shown in Figure 18 and the measured performance. The P1dB was measured to be better than 38 dBm in the frequency band of 2050 MHz to 2250 MHz.

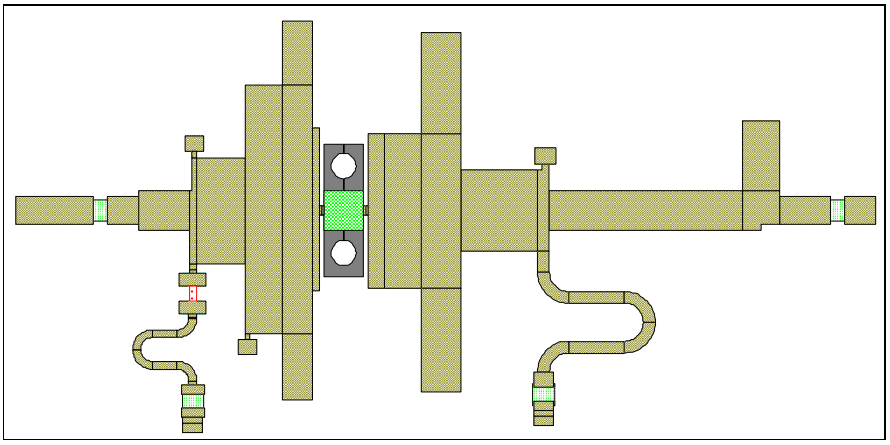

Figure 18. Final RF layout

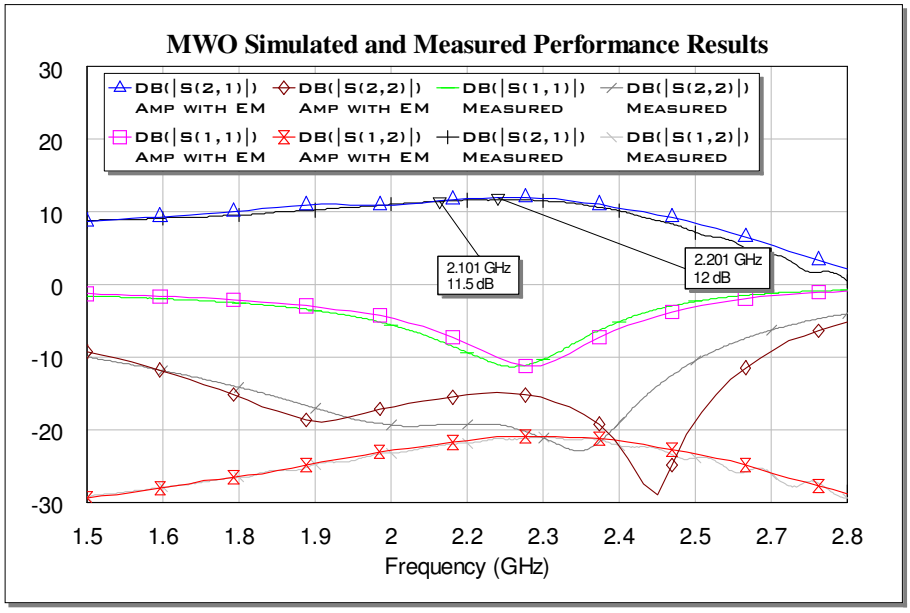

Figure 19. Comparison between simulated and measured performance

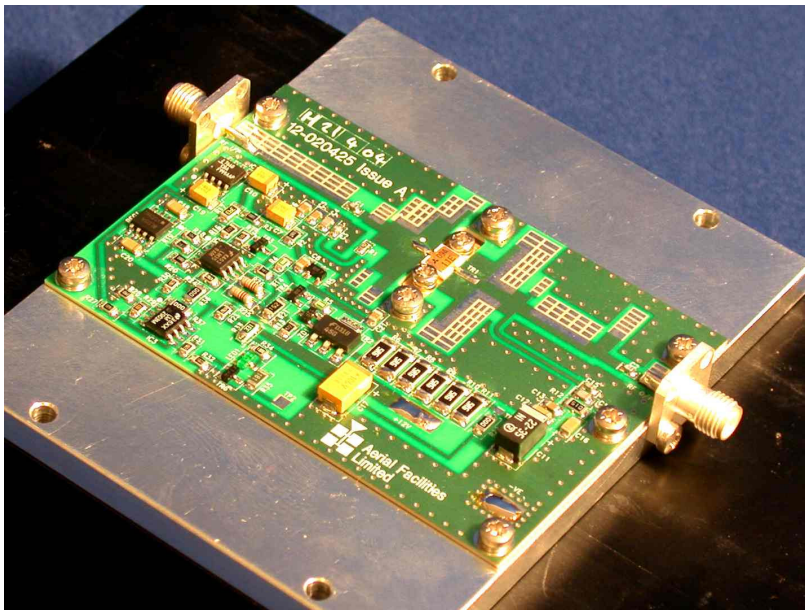

Figure 20. Test unit

The comparison between the measured performance of the first test unit (just after switching on the power supply) and the simulated performance decisively indicate that the design method and procedure described in this paper lead to f*irst-time-right* designs of linear power amplifiers.

Design comments and tips

The gain and the return loss are centred somewhat above the design frequency band of 2.1-2.2 GHz. That was done intentionally during the design phase because experience has shown that the combined effect of the tolerances of the parameters of the components, the production tolerances and even design faults is such that the performance always slips towards lower frequencies. This time it

didn't, but experience has also shown that tuning towards lower frequencies is easier and does not lead to loss of performance, while tuning towards higher frequencies is very often a headache.

The output return loss of the manufactured amplifier is quite good. An inexperienced RF amplifier designer may believe that if the amplifier is designed for good input and output match (again by using only the *S-parameters*) the amplifier will also deliver maximum P1dB. That misconception is still floating around although it was thoroughly discussed by Cripps in [4]. It is very easy to use *MultiMatch* and its *Power Parameters* analysis capabilities to simultaneously display the load-pull constant power contours and the constant maximum gain circles (Figure 21) on a Smith Chart. In Figure 21, the constant power contours are spaced by 1 dB and the constant gain circles by 0.5 dB. It is obvious that if the transistor is matched for maximum gain the P1dB will be about 3 dB less than the maximum possible.

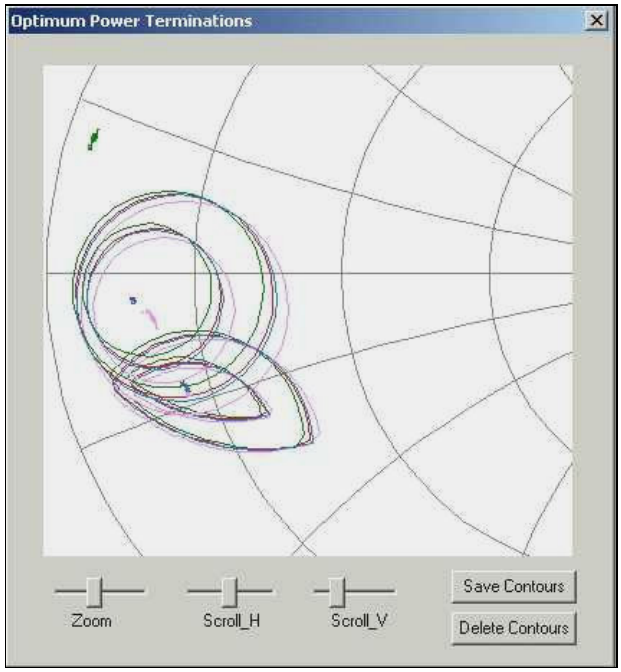

Figure 21. Constant power contours and constant gain circles

Summary and conclusions

A procedure for designing RF/microwave linear (Class A) power amplifiers was described where the only data initially used is the small-signal *S-parameters* of the transistors. The method of design is to use the *MultiMatch Amplifier Design Wizard* with its innovative *Power Parameters* and powerful network synthesis capabilities to design for the desired P1dB, operational gain and frequency band. *Microwave Office* with its EM layout simulator is used in conjunction with *MultiMatch* to accurately simulate the discontinuities of the matching networks and to fine tune the networks to reduce these effects.

References

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